IN THE CLAIMS

[cancelled by "a"] Please cancel claims 21-30 without prejudice.

Please amend the following claims:

M.G

1. (AMENDED) A method of forming a passivation layer [on a semiconductor substrate, said method] comprising [the steps of]:

forming a first dielectric layer over a metal interconnect layer [on] above a semiconductor substrate, said metal interconnect layer including a bond pad and a metal member spaced apart from said bond pad by a gap, said first dielectric layer formed over said bond pad and said metal member and in said gap, wherein said first dielectric layer is at least as thick as said metal layer and said gap between said bond pad and said metal member is completely filled by said first dielectric layer said first dielectric having a dielectric constant at least as low as silicon dioxide;

C1

forming a second dielectric layer over said first dielectric layer said second dielectric being hermetric;

forming an opening to expose the top surface of said bond pad, wherein the sidewalls of said opening expose the edges of said second dielectric layer and said first dielectric layer; and

forming a conducting barrier layer over said second dielectric layer, over sidewalls of said opening, and over said exposed top surface of said bond pad to form a continuous seal.

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2. (AMENDED) The method of claim 1 wherein [said second dielectric layer and] said barrier layer [are] is resistant to moisture penetration.

C2

6. (AMENDED) A method of forming a hermetically sealed integrated circuit[, said method] comprising [the steps of]:

forming a first dielectric layer over a bond pad on a semiconductor substrate said first dielectric layer having a first dielectric constant;

forming a second dielectric layer over said first dielectric layer said second dielectric being hermetic and having a second dielectric constant, said second dielectric constant greater than said first dielectric contant;

forming an opening to expose the top surface of said bond pad, wherein the sidewalls of said opening expose the edges of said second dielectric layer and said first dielectric layer;

forming a conducting barrier layer over said second dielectric layer, over sidewalls of said opening, and over said exposed top surface of said bond pad to form a continuous seal, wherein said second dielectric layer and said barrier layer are resistant to moisture penetration, and

forming a bump on said barrier layer in said opening.

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11 (Amended) A method of forming a low interconnect capacitance wafer passivation[, said method] comprising [the steps of]:

forming a metal interconnect layer having a first member spaced apart from a second member by a gap;

forming a first dielectric layer over said first and second members and in said gap, wherein said first dielectric layer is at least as thick as said metal layer and said gap between said members is completely filled by said first dielectric layer;

forming a second dielectric layer over said first dielectric layer, wherein second dielectric layer has a larger dielectric constant than said first dielectric layer;

forming an opening to expose the top surface of at least one of said spaced apart members, wherein the sidewalls of said opening expose the edges of said second dielectric layer and said first dielectric layer;

forming a conducting barrier layer over said second dielectric layer, over sidewalls of said opening, and over said exposed top surface of at least one of said spaced apart members to form a continuous seal, wherein said second dielectric layer and said barrier layer are resistant to moisture penetration, and

forming a contact on said barrier layer in said opening.

C 3 (concluded)

12. (amended) The method of claim 11 further comprising [the step of]:

forming a third dielectric layer over said second dielectric layer prior to forming an opening to expose the top surface of at least one of said spaced apart members.